Claim Amendments

1. (Previously Presented) An electronic system comprising:

a first memory module having a first memory array and a first buffer logic coupled to the first memory array;

a second memory module having a second memory array and a second buffer logic coupled to the second memory array; and

an analysis module having a third buffer logic and an analysis device coupled to the third buffer logic, wherein the analysis module is interposed between the second buffer logic and the first buffer logic,

wherein the second buffer logic transmits a test pattern through the third buffer logic to the first buffer logic to carry out a test of the first memory module independently of a memory controller, and the analysis device analyzes a result of the test transmitted by the first buffer logic.

2. (Previously Presented) The electronic system of claim 1, further comprising:

the memory controller coupled to the second buffer logic; and

a processor coupled to the memory controller to execute instructions stored in the second memory array of the second memory module under the control of the memory controller.

3. (Original) The electronic system of claim 2, wherein the memory controller transmits a command to the second buffer logic under the control of the processor to cause the second buffer logic to carry out a test of the first memory module.

4. (Original) The electronic system of claim 3, further comprising a memory bus coupling together the memory controller, the first memory module and the second memory module, and wherein the test pattern is transmitted across the memory bus.

5. (Canceled).

6. (Original) The electronic system of claim 1, further comprising a test source coupled to the second buffer logic, wherein the test source transmits a command to the second buffer logic to cause the second buffer logic to carry out a test of the first memory module.

7. (Original) The electronic system of claim 6, further comprising a serial bus coupling the second buffer logic to the test source, wherein the command is transmitted by the test source across the serial bus to the second buffer logic.

8. (Original) The electronic system of claim 6, wherein the test pattern is received by the second buffer logic from the test source and wherein the second buffer

logic stores the test pattern in the second memory array in preparation for transmitting the test pattern to the first buffer logic of the first memory module.

9. (Original) The electronic system of claim 1, wherein the test pattern is generated by the second buffer logic in response to commands received by the second buffer logic and wherein the second buffer logic stores the test pattern in the second memory array in preparation for transmitting the test pattern to the first buffer logic of the first memory module.

10. (Previously Presented) The electronic system of claim 1, wherein the test pattern incorporates commands for the first buffer logic to carry out.

11. (Previously Presented) The electronic system of claim 1, wherein the test pattern incorporates a deliberately created error to elicit an expected action on the part of the first memory module upon encountering the deliberately created error.

12. (Canceled).

13. (Previously Presented) The electronic system of claim 1, further comprising:

a first point-to-point bus coupling the first buffer logic of the first memory module to the third buffer logic; and

a second point-to-point bus coupling the second buffer logic of the second memory module to the third buffer logic.

14. (Previously Presented) The electronic system of claim 1, wherein the third buffer logic provides an indication to the analysis device of the transmission of the test pattern by the second buffer logic to the first buffer logic, and wherein the third buffer logic provides an indication to the analysis device of a signal transmitted by the first buffer logic in response to the carrying out of a test by the second buffer logic and indicating a status of the test.

15. (Previously Presented) The electronic system of claim 1, wherein all three of the first buffer logic, the second buffer logic and the third buffer logic are integrated circuits of substantially similar design, and wherein the interface of the third buffer logic to couple the third buffer logic to the analysis device is of substantially the same design as both a corresponding interface of the first buffer logic to couple the first buffer logic to the first memory array, and a corresponding interface of the second buffer logic to couple the second buffer logic the second memory array.

16-31. (Canceled).